IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Bruce B. Doris, et al.

Docket No.: FIS920030246

Serial No.: 10/701,526

Group Art Unit: 2811

Filed: November 6, 2003

Examiner: Gebremariam, S.

For: **HIGH MOBILITY CMOS CIRCUITS**

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

DECLARATION UNDER 37 C.F.R. §1.131

Sir:

We, Bruce B. Doris, Oleg G. Gluschenkov and Huilong Zhu, do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1, 11, 20 and 23 (and the claims dependent therefrom) of the above-identified application.

2. We completed the invention of claims 1, 11, 20 and 23 (and those claims dependent therefrom) in the United States before November 4, 2003, as evidenced below.

CONCEPTION

3. Before November 4, 2003, we conceived of a method and apparatus which utilizes selectively applied thin stressed films, such as tensile films, thick compressive films and thick tensile films, to enhance electron and hole mobility in CMOS circuits, as disclosed in the above-identified application and recited in at least independent claims 1, 11, 20 and 23 (and dependent claims therefrom) of the application, of which is evidenced by IBM Disclosure FIS8-2003-0283 (hereinafter referred to as the Invention Disclosure)

attached hereto as Exhibit A. The Invention Disclosure attached hereto is a photocopy of and is identical to the original, except that all pertinent dates have been removed therefrom.

4. All pertinent dates removed from the Invention Disclosure attached hereto are before November 4, 2003.

5. As evidenced in the Invention Disclosure, the semiconductor structure includes:

a. a plurality of field effect transistors having a first portion of field effect transistors (FETS) and a second portion of field effect transistors;

b. a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

c. a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

6. As further evidenced in the Invention Disclosure, the semiconductor structure formed on a substrate includes:

a. a first plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a first defined spacing range;

b. a second plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a second defined spacing range;

c. a first plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a third defined spacing range;

d. a second plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a fourth defined spacing range;

e. a first tensile layer having a first tensile layer thickness and being configured to impart a first determined tensile stress to the first plurality of n-channel field effect transistors;

f. a second tensile layer having a second tensile layer thickness and being configured to impart a second determined tensile stress to the second plurality of n-channel field effect transistors;

g. a first compressive layer having a first compressive layer thickness and being configured to impart a first determined compressive stress to the first plurality of p-channel field effect transistors; and

h. a second compressive layer having a second compressive layer thickness and being configured to impart a second determined compressive stress to the second plurality of p-channel field effect transistors.

7. As further evidenced in the Invention Disclosure, the method of forming a semiconductor structure includes:

a. forming a plurality of field effect transistors on a semiconductor substrate, the plurality of field effect transistors including a first portion of field effect transistors and a second portion of field effect transistors;

b. depositing a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

c. depositing a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

8. As further evidenced in the Invention Disclosure, the semiconductor includes:

a. a plurality of field effect transistors formed on the substrate, the plurality of field effect transistors including a first portion of field effect transistors and a second position of filed effect transistors;

b. a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

c. a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

9. The benefits and features of the invention are shown and described in the Invention Disclosure.

DUE DILIGENCE

10. Prior to November 4, 2003, the inventors submitted the Invention Disclosure to IBM counsel for review and preparation of a patent application.

11. Prior to November 4, 2003, IBM counsel conveyed the Invention Disclosure to patent counsel at McGuireWoods, LLP for preparation of a patent application.

12. Prior to the filing of the present application in the U.S. Patent Office, McGuireWoods counsel prepared a draft application and sent the draft to Inventor Doris. Inventor Doris communicated with patent counsel at McGuireWoods LLP, on behalf of all of the inventors, in perfecting a patent application based on the Invention Disclosure. For example, communications took place at least on October 10, 2003, October 20, 2003, October 21, 2003 and October 23, 2003 when a final application was completed encompassing the invention as described in the attached Invention Disclosure.

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15. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Bruce B. Doris	Date
Oleg G. Gluschenkov O.G.	3/4/05 Date
Huilong Zhu	Date

\\COM\487796.1

Disclosure FIS8-2003-0283

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Bruce Doris On
Last Modified By Bruce Doris

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
HIGH MOBILITY CMOS CIRCUITS

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(KBG) KBG ... CHEN: CMOS-6X/HPLS
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Submitted Date		
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: Bruce Doris/Fishkill/IBM, Oleg Gluschenkov/Fishkill/IBM, Huilong Zhu/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Doris, Bruce B.	216146	29/UX3A	532-3681	Ieong, Meikei
Gluschenkov, Oleg G.	2A1177	29/BIXA	892-9788	Sekiguchi, Akihisa (Aki)
Zhu, Huilong	6A2510	29/62GD	532-9641	Oldiges, Philip (Phil)

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Response Due to IP&L	

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Conventional CMOS scaling is becomming more challenging, in part, due to the physical limitations of such elements as gate oxide thickness and junction depth. One potential soultion is to introduce new device archetectures to enhance charge carrier mobility. The most common approach to mobility enhancement is to grow a strained Si layer ontop of a relaxed SiGe buffer layer. However, significant challenges exist for this technology. For example, pFET performance improvents require concentrations of Ge in excess of 30% which may increase defect density. Other methodologies are actively being persued to enhance mobility. One broad category of mobility enhancement techniques is local mechanical stress. Experimentally it has been observed that electron mobility can be improved by imparting tensile stress either along the current flow or orthogonal to the current flow, and hole mobility is enhanced by imparting compressive stress along the current flow and tensile stress perpindicular to the current flow.

One method of imparting tensile stress to the nFET channel is to apply a tensile etch stop layer. Compressive stress may be imparted to the pFET channel by applying a compressive etch stop film. One problem with this approach is that the compressive film degrades the nFET and the tensile film degrades the pFET. Another problem with this approach is that although films with significant stress are available, the thickness of these films are limited to about 300A or less in a dense structure like a cache or SRAM cell. Since gates are spaced ata a minimum pitch, a void is created in the film if the film is too thick. This main problem with this is that the voids are opened up during the contact etch process and fill with contact metal. Since the voids run parallea to the gates, the contact metal fills the voids and causes contact shorts which prevent proper circuit functionality.

On the other hand, it is highly advantageous to have a very thick etch stop film because film thickness is directly proportional to the stress that can be imparted to the channel. This invention is aimed at producing a plurality of circuits haveing varying etch stop layer thickness for the purpose of improving mobility in selected circuits or circuit elements. The invention specifies a range of film thicknesses based on the distance between gate features.

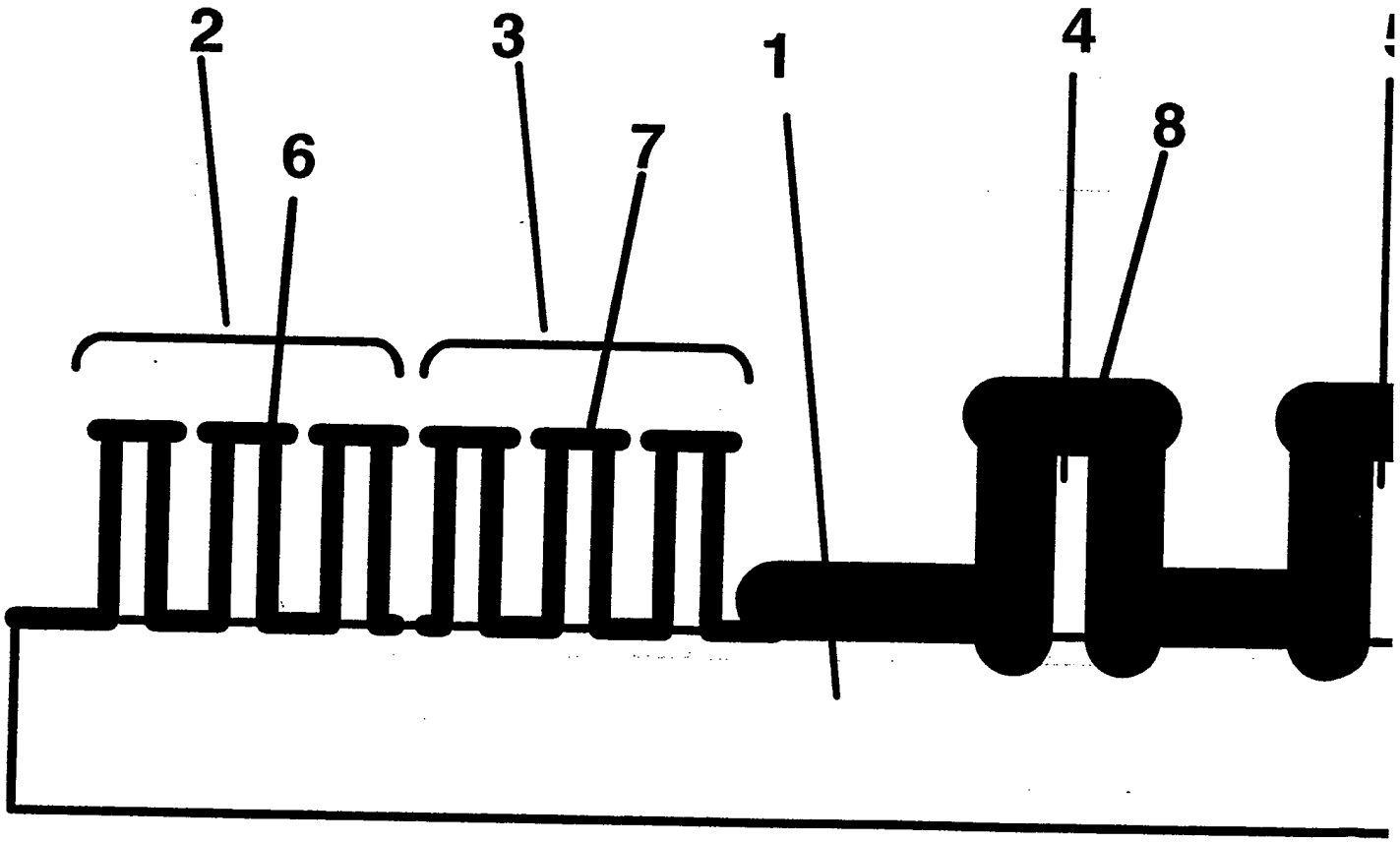
This invention has broad claims that may be detected using standard failure analysis techniques.

Several methods may be used to obtain the described structure. One such method involves fabricating FETs on a substrate 1. Next, depositing a thin tensile film 6 for one class of nFETs 2 having a minimum spacing. An oxide liner layer, not shown in the figure, is next deposited over the wafer. The thin tensile film 6 is next masked on the locations where the dense nFETs 6 are present, and removed from everywhere else on the wafer. The mask is removed selectively. An oxide liner layer is deposited over the entire wafer followed by deposition of a thin compressive film 7. A mask is used to protect the thin compressive film 7

over the dense pFETs. The compressive film 7 is then removed from the unmasked regions, and the mask is then removed selectively with respect to all other materials. A thin oxide liner layer is next deposited over the wafer. Next, a thick tensile film 8 is deposited over the entire wafer. A mask is next applied to protect the isolated nFET regions, 4 while exposing the rest of the wafer. The thick tensile film is then removed from the exposed regions and the mask material is then removed. Finally a thin oxide layer is deposited over the wafer followed by the deposition of a thick compressive film 9. A mask is patterned over the isolated pFET regions 5, and the thick compressive film is removed from the unmasked regions of the wafer. The mask material is then removed.

This method may be repeated to enable FETs with different spacing to have films of different thicknesses. In a preferred embodiment, nFETs in a densley populated region have a thin tensile film, while pFETs on a densly poplulated region have a thin compressive film. On the same chip, nFETs having larger than minimum spacing will have a thick tensile film while pFETs in a less than minimum spaces region will have a thick compressive film.

The final device structure appears a follows:



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6. As further evidenced in the Invention Disclosure, the semiconductor structure formed on a substrate includes:

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b. a second plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a second defined spacing range;

c. a first plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a third defined spacing range;

d. a second plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a fourth defined spacing range;

e. a first tensile layer having a first tensile layer thickness and being configured to impart a first determined tensile stress to the first plurality of n-channel field effect transistors;

f. a second tensile layer having a second tensile layer thickness and being configured to impart a second determined tensile stress to the second plurality of n-channel field effect transistors;

g. a first compressive layer having a first compressive layer thickness and being configured to impart a first determined compressive stress to the first plurality of p-channel field effect transistors; and

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7. As further evidenced in the Invention Disclosure, the method of forming a semiconductor structure includes:

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Bruce B. Doris	Date
Oleg G. Gluschenkov	Date
Huilong Zhu	03/02/2005 Date

\\COM\487796.1

Disclosure FIS8-2003-0283

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Bruce Doris On
Last Modified By Bruce Doris

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
HIGH MOBILITY CMOS CIRCUITS

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(KBG) KBG ... CHEN: CMOS-6X/HPLS
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Submitted Date		
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: Bruce Doris/Fishkill/IBM, Oleg Gluschenkov/Fishkill/IBM, Huilong Zhu/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
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***Main Idea**

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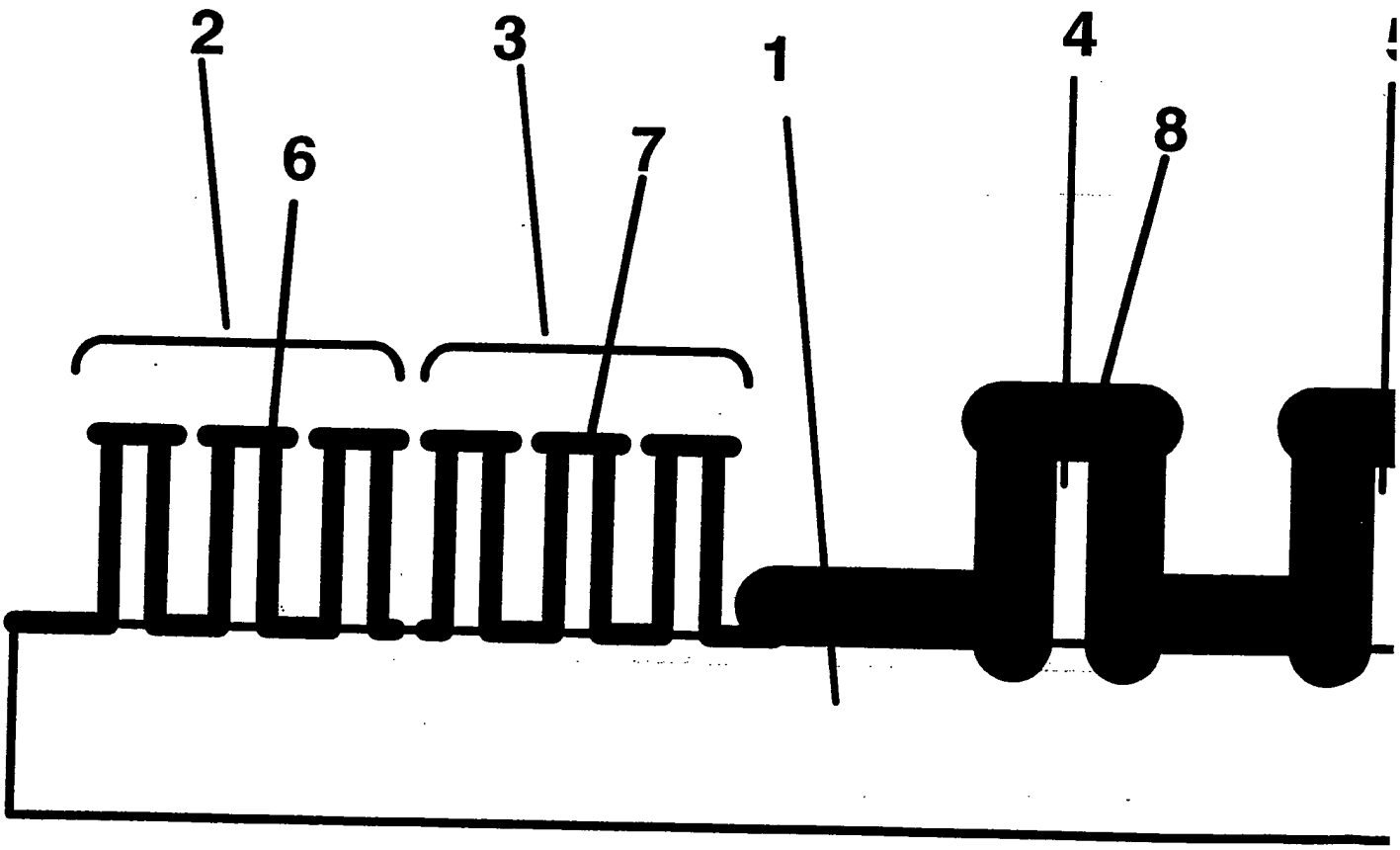

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12. Prior to the filing of the present application in the U.S. Patent Office, McGuireWoods counsel prepared a draft application and sent the draft to Inventor Doris. Inventor Doris communicated with patent counsel at McGuireWoods LLP, on behalf of all of the inventors, in perfecting a patent application based on the Invention Disclosure. For example, communications took place at least on October 10, 2003, October 20, 2003, October 21, 2003 and October 23, 2003 when a final application was completed encompassing the invention as described in the attached Invention Disclosure.

13. During this time and prior to November 4, 2003, we worked diligently on providing information to IBM in-house counsel and counsel at McGuireWoods, and preparing the patent application for filing in the U.S. Patent Office. All of the inventors were involved in reviewing and finalizing the application for the present invention prior to the filing of the above-identified application.

14. We worked diligently on the preparation of the patent application with patent counsel at McGuireWoods until a final draft patent application was completed to our satisfaction. A final draft was forwarded to us by McGuireWoods counsel Andrew M. Calderon on October 23, 2003, who filed the application, on our behalf, on November 6, 2003. At all times, we worked diligently to finalize the application for filing in the U.S. Patent and Trademark Office from prior to November 4, 2003 to the finalized application on November 6, 2003.

15. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Bruce B. Doris — Date: 2/24/05

Oleg G. Gluschenkov — Date:

Huilong Zhu — Date:

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Disclosure FIS8-2003-0283

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Bruce Doris On
Last Modified By Bruce Doris

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
HIGH MOBILITY CMOS CIRCUITS

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(KBG) KBG ... CHEN: CMOS-6X/HPLS
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Submitted Date		
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

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Response Due to IP&L	

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Conventional CMOS scaling is becomming more challenging, in part, due to the physical limitations of such elements as gate oxide thickness and junction depth. One potential soultion is to introduce new device archetectures to enhance charge carrier mobility. The most common approach to mobility enhancement is to grow a strained Si layer ontop of a relaxed SiGe buffer layer. However, significant challenges exist for this technology. For example, pFET performance improvents require concentrations of Ge in excess of 30% which may increase defect density. Other methodologies are actively being persued to enhance mobility. One broad category of mobility enhancement techniques is local mechanical stress. Experimentally it has been observed that electron mobility can be improved by imparting tensile stress either along the current flow or orthogonal to the current flow, and hole mobility is enhanced by imparting compressive stress along the current flow and tensile stress perpindicular to the current flow.

One method of imparting tensile stress to the nFET channel is to apply a tensile etch stop layer. Compressive stress may be imparted to the pFET channel by applying a compressive etch stop film. One problem with this approach is that the compressive film degrades the nFET and the tensile film degrades the pFET. Another problem with this approach is that although films with significant stress are available, the thickness of these films are limited to about 300A or less in a dense structure like a cache or SRAM cell. Since gates are spaced ata a minimum pitch, a void is created in the film if the film is too thick. This main problem with this is that the voids are opened up during the contact etch process and fill with contact metal. Since the voids run parallea to the gates, the contact metal fills the voids and causes contact shorts which prevent proper circuit functionality.

On the other hand, it is highly advantageous to have a very thick etch stop film because film thickness is directly proportional to the stress that can be imparted to the channel. This invention is aimed at producing a plurality of circuits haveing varying etch stop layer thickness for the purpose of improving mobility in selected circuits or circuit elements. The invention specifies a range of film thicknesses based on the distance between gate features.

This invention has broad claims that may be detected using standard failure analysis techniques.

Several methods may be used to obtain the described structure. One such method involves fabricating FETs on a substrate 1. Next, depositing a thin tensile film 6 for one class of nFETs 2 having a minimum spacing. An oxide liner layer, not shown in the figure, is next deposited over the wafer. The thin tensile film 6 is next masked on the locations where the dense nFETs 6 are present, and removed from everywhere else on the wafer. The mask is removed selectively. An oxide liner layer is deposited over the entire wafer followed by deposition of a thin compressive film 7. A mask is used to protect the thin compressive film 7

over the dense pFETs. The compressive film 7 is then removed from the unmasked regions, and the mask is then removed selectively with respect to all other materials. A thin oxide liner layer is next deposited over the wafer. Next, a thick tensile film 8 is deposited over the entire wafer. A mask is next applied to protect the isolated nFET regions, 4 while exposing the rest of the wafer. The thick tensile film is then removed from the exposed regions and the mask material is then removed. Finally a thin oxide layer is deposited over the wafer followed by the deposition of a thick compressive film 9. A mask is patterned over the isolated pFET regions 5, and the thick compressive film is removed from the unmasked regions of the wafer. The mask material is then removed.

This method may be repeated to enable FETs with different spacing to have films of different thicknesses. In a preferred embodiment, nFETs in a densley populated region have a thin tensile film, while pFETs on a densly poplulated region have a thin compressive film. On the same chip, nFETs having larger than minimum spacing will have a thick tensile film while pFETs in a less than minimum spaces region will have a thick compressive film.

The final device structure appears a follows: